



## SSC8334GSB

### Dual N-Channel Enhancement MOSFET

#### ➤ Features

VDS	VGS	RDSON Typ.	ID	ESD
30V	±12V	450mR@4V5	1A	1.2KV
		520mR@2V5		

#### ➤ Description

SSC8334GSB uses advanced trench technology to provide excellent RDSON and low gate charge. The complementary MOSFETS may be used to form a level shifted high side switch, and for a host of other applications.

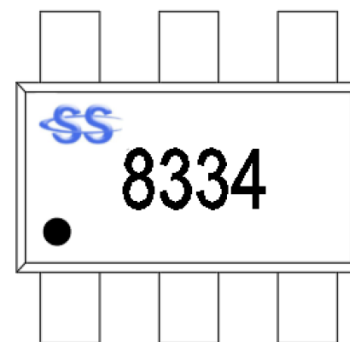
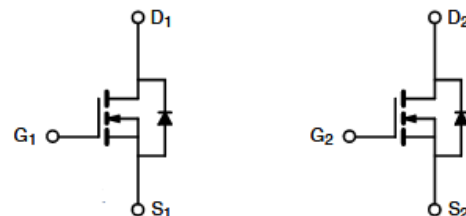
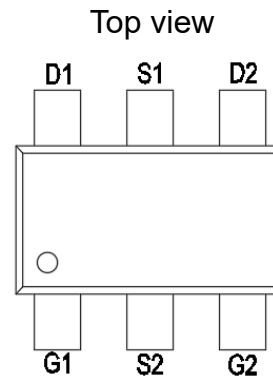
#### ➤ Applications

- Small signal switch
- Load switch
- Digital Transistors

#### ➤ Ordering Information

Device	Package	Shipping
SSC8334GSB	SOT23-6L	3000/Reel

#### ➤ Pin configuration



Marking



➤ **Absolute Maximum Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DSS}$	Drain-to-Source Voltage	30	V
$V_{GSS}$	Gate-to-Source Voltage	$\pm 12$	V
$I_D$	Continuous Drain Current <sup>a</sup>	1	A
$I_{DM}$	Pulsed Drain Current <sup>b</sup>	3	A
$P_{DSM}$	Power Dissipation <sup>a</sup>	0.8	W
$P_D$	Power Dissipation <sup>c</sup>	0.3	W
$T_J$	Operation junction temperature	-55 to 150	$^{\circ}\text{C}$
$T_{STG}$	Storage temperature range	-55 to 150	$^{\circ}\text{C}$

➤ **Thermal Resistance Ratings**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

Symbol	Parameter	Typical	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>a</sup>	420	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC}$	Junction-to-Case Thermal Resistance	160	

Note:

- The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in<sup>2</sup> FR-4 board with 2oz.copper,in a still air environment with  $T_A=25^{\circ}\text{C}$ .The value in any given application depends on the user is specific board design. The current rating is based on the  $t \leq 10\text{s}$  thermal resistance rating.
- Repetitive rating, pulse width limited by junction temperature.
- The power dissipation  $P_D$  is based on  $T_{J(MAX)}=150^{\circ}\text{C}$ , using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heat sinking is used.

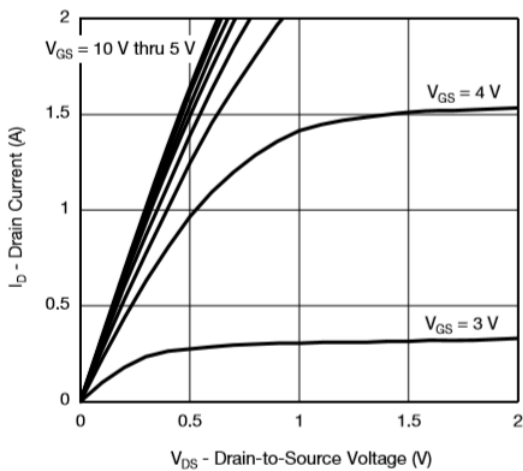


➤ **Electronics Characteristics**( $T_A=25^{\circ}\text{C}$  unless otherwise noted)

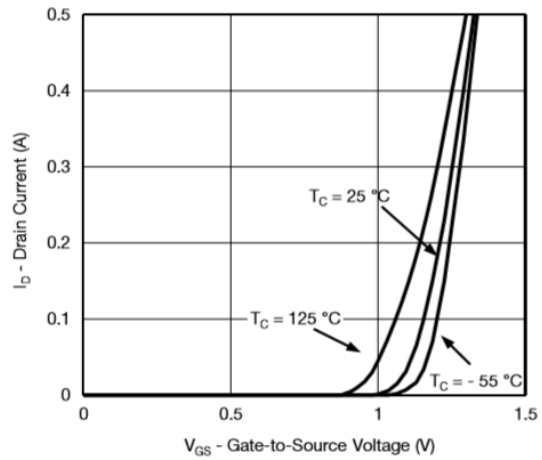
Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.6	1	1.3	V
$R_{DS(on)}$	Drain-Source On- Resistance	$V_{GS}=4.5V, I_D=1A$		450	700	mR
		$V_{GS}=2.5V, I_D=1A$		520	900	
		$V_{GS}=1.8V, I_D=0.5A$		950	1500	
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=24V, V_{GS}=0V$			1	$\mu A$
$I_{GSS}$	Gate-Source leak current	$V_{GS}=\pm 10V, V_{DS}=0V$			$\pm 10$	$\mu A$
$G_{FS}$	Transconductance	$V_{DS}=5V, I_D=1A$		1		S
$V_{SD}$	Forward Voltage	$V_{GS}=0V, I_S=1A$		0.9	1.3	V
$C_{iss}$	Input Capacitance	$V_{DS}=15V, V_{GS}=0V,$ $f=1MHz$		62		pF
$C_{oss}$	Output Capacitance			16		
$C_{rss}$	Reverse Transfer Capacitance			4		
$Q_g$	Total Gate Charge	$V_{DS}=15V, V_{GS}=4.5V,$ $I_D=3.8A$		1		nC
$Q_{gs}$	Gate Source Charge			0.3		
$Q_{gd}$	Gate Drain Charge			0.2		
$T_{D(ON)}$	Turn-on delay time	$V_{DS}=15V, V_{GS}=6V,$ $R_L=30R, R_{GEN}=1R$		3		ns
$T_r$	Rise time			14		
$T_{D(OFF)}$	Turn-off delay time			11		
$T_f$	Fall time			9		



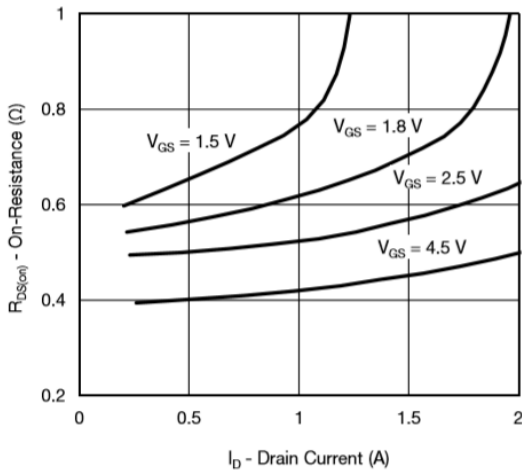
➤ **N-Channel Typical Characteristics**( $T_A=25^\circ\text{C}$  unless otherwise noted)



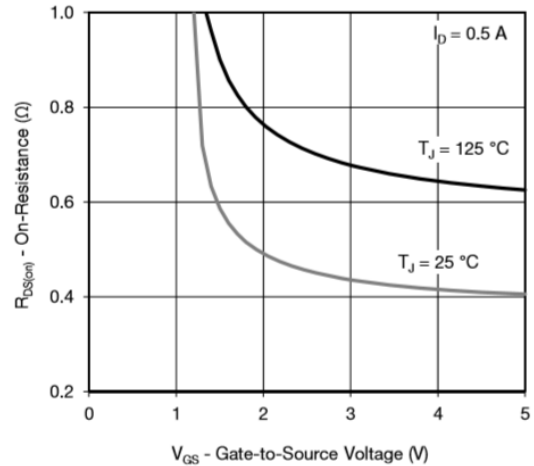
**Output Characteristics**



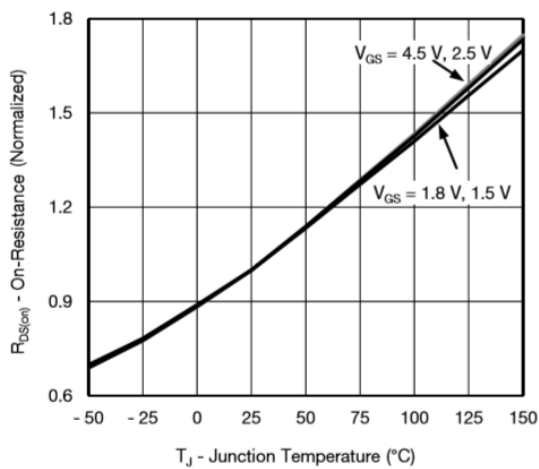
**Transfer Characteristics**



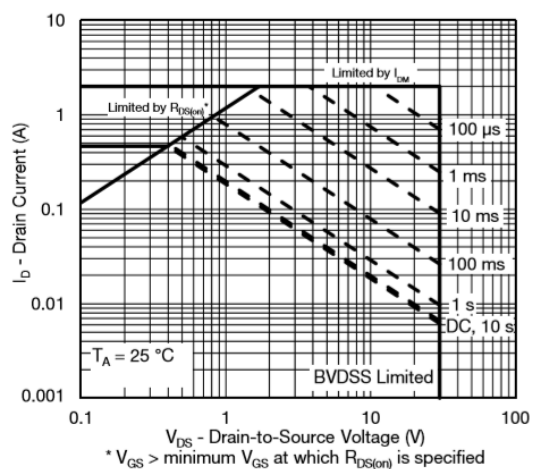
**On-Resistance vs. Drain Current**



**On-Resistance vs. Gate-to-Source Voltage**



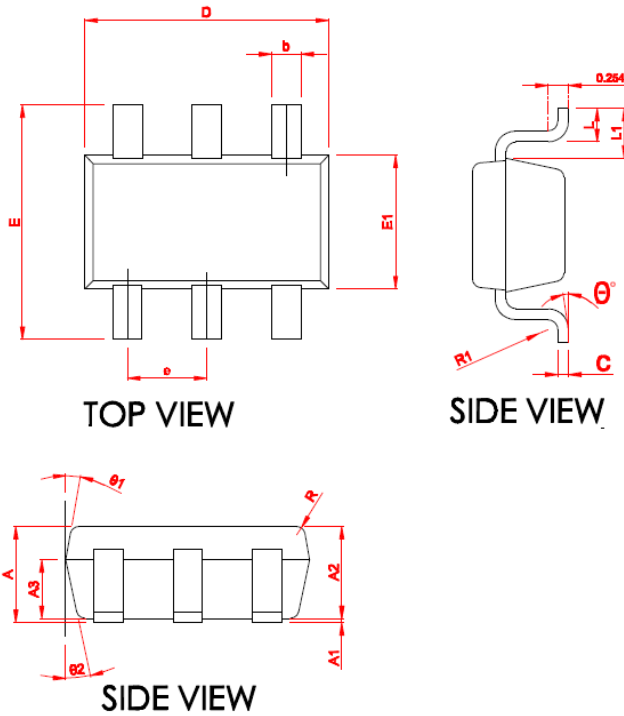
**On-Resistance vs. Junction Temperature**



**Safe Operating Area, Junction-to-Ambient**



➤ Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.06	1.15	1.24
* A1	0.01	0.05	0.09
* A2	1.05	1.10	1.15
A3	0.65	0.70	0.75
* b	0.30	0.35	0.45
* c	0.117	0.127	0.157
* D	2.87	2.92	2.97
* E	2.72	2.80	2.88
* E1	1.55	1.60	1.65
* e	0.90	0.95	1.00
* L	0.32	0.40	0.48
* L1	0.55	0.60	0.65
R	0.10 REF		
R1	0.12 REF		
* $\theta$	0	--	8°
$\theta_1$	8°	10°	12°
$\theta_2$	10°	12°	14°

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